Amendments to the Claims

Please amend the claims as follows:

1-65. (canceled)

66. (original) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon-comprising ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

67. (original) The capacitor of Claim 66, wherein the nanostructures comprise a silicon oxycarbide ceramic.

68. (original) The capacitor of Claim 66, wherein the nanostructures are in the form of porous structures.

69. (original) The capacitor of Claim 66, wherein the nanostructures are in the form of relief structures.

70. (original) The capacitor of Claim 69, wherein the nanostructures are in the form of struts.

71. (original) The capacitor of Claim 66, wherein the nanostructures are formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

72. (original) The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

73. (original) The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

74. (original) The capacitor of Claim 71, wherein the hydrocarbon block comprises polyisoprene, and the silicon-comprising block comprises poly(pentamethyldisilylstyrene).

75. (original) The capacitor of Claim 71, wherein the polymeric material comprises poly(dimethylsiloxane).

76. (original) The capacitor of Claim 66, wherein the dielectric layer comprises silicon nitride.

77. (original) The capacitor of Claim 66, wherein the upper capacitor electrode comprises a doped polysilicon.

78. (original) The capacitor of Claim 66, wherein the upper capacitor electrode comprises a conductive metal.

79. (original) The capacitor of Claim 66, wherein the capacitor is integrated into a DRAM cell.

80. (original) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

81. (original) The capacitor of Claim 80, wherein the nanostructures are in the form of porous structures.

82. (original) The capacitor of Claim 80, wherein the nanostructures are in the form of relief structures.

83. (original) The capacitor of Claim 82, wherein the nanostructures are in the form of struts.

84. (original) The capacitor of Claim 83, wherein the nanostructures comprise an ultraviolet irradiated and ozonolyzed polymeric material comprising a hydrocarbon block and a silicon-containing block.

85. (original) The capacitor of Claim 80, wherein the capacitor is integrated into a DRAM cell.

86. (original) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

87. (original) The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

88. (original) The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

89-129. (canceled)

130-150. (canceled)

151. (original) A semiconductor circuit, comprising a capacitor;

the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic and formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

152. (original) The semiconductor circuit of Claim 151, wherein the nanostructures form a periodic network, and the overlying conductive layer comprises an ordered array of island clusters.

153. (original) The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of porous structures.

154. (original) The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of relief structures.

155. (original) The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises doped amorphous silicon, pseudo-crystalline silicon, or polycrystalline silicon.

156. (original) The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises a conductive metal.

157. (canceled)

158. (original) An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array, the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

159. (canceled)

160. (amended) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an ordered array of nanostructures of substantially uniform size, and the texturizing layer comprising a polymeric material;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

161. (canceled)

162. (amended) The capacitor of Claim ~~161~~ 160, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

163. (previously presented) The capacitor of Claim 162, wherein the polymeric material comprises polyisoprene and poly(pentamethyldisilylstyrene).

164-167. (canceled)

168. (previously presented) The capacitor of Claim 160, wherein the texturizing layer comprises a plurality of two-dimensional structures.

169. (amended) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising a periodic network of surface structures having a substantially uniform height, and the texturizing layer comprising a polymeric material;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

170. (amended) A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an ordered array of nanostructures of substantially uniform dimensions, and the texturizing layer comprising a polymeric material;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

171. (previously presented) A semiconductor circuit, comprising a capacitor according to Claim 160.

172. (canceled)

173. (amended) The circuit of Claim ~~172~~ 171, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

174-176. (canceled)

177. (previously presented) A semiconductor circuit, comprising a capacitor according to Claim 169.

178. (previously presented) A semiconductor circuit, comprising a capacitor according to Claim 170.

179. (previously presented) An integrated circuit, comprising:
an array of memory cells;
internal circuitry; and
at least one capacitor according to Claim 160, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

180. (canceled)

181. (amended) The circuit of Claim ~~180~~ 179, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

182-184. (canceled)

185. (previously presented) An integrated circuit, comprising:
an array of memory cells;
internal circuitry; and
at least one capacitor according to Claim 169, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

186. (previously presented) An integrated circuit, comprising:
an array of memory cells;
internal circuitry; and
at least one capacitor according to Claim 170, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

187. (previously presented) An integrated circuit supported by a substrate, and comprising a capacitor according to Claim 66.

188. (canceled)

189. (previously presented) An integrated circuit supported by a substrate, and comprising a capacitor according to Claim 160.

190. (previously presented) A lower capacitor electrode, produced by the process of:

depositing a polymeric material comprising a hydrocarbon block and a silicon-containing block onto an insulative layer; and exposing the polymer material to ozone and electromagnetic radiation to form a texturizing layer comprising an ordered array of nanostructures of substantially uniform size; and

forming a conductive layer over the texturizing layer.

191. (previously presented) The electrode of Claim 190, wherein the polymeric material comprises a triblock copolymer of the type A_1BA_2, where the "A" copolymer is the hydrocarbon block and the "B" copolymer is the silicon-containing block.

192. (previously presented) The electrode of Claim 190, wherein the polymeric material comprises polyisoprene and poly(pentamethyldisilylstyrene).

193-196. (canceled)

197. (amended) A lower capacitor electrode, produced by the process of:

depositing a polymeric texture-forming material onto an insulating layer;

forming the material into an ordered array of nanostructures of substantially uniform dimensions; and

depositing a conductive layer onto the nanostructures.

198. (previously presented) A capacitor, produced by the process of:

depositing a silicon-comprising hydrocarbon polymeric material into an opening in an insulating layer, and exposing the polymeric material to ultraviolet radiation and ozone to form a texturizing layer comprising silicon oxycarbide ceramic nanostructures;

forming a conductive layer over the texturizing layer to form a lower capacitor electrode;

forming a dielectric layer over the lower capacitor electrode; and

forming an upper capacitor electrode over the dielectric layer.

199-203. (canceled)